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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/080,568 | 02/25/2002 | Stephen M. Gates | YOR919980324 US2 | 9141 |

21254 7590 03/27/2003

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|---|
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| ART UNIT | PAPER NUMBER |
|---|---|
| 2814 | |

DATE MAILED: 03/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 10/080,568 | Applicant(s) GATES ET AL. | |
|---|---|---|---|
| | Examiner Phat X. Cao | Art Unit 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *11-18 and 26-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-18 and 26-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. Claims 15-16 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

- In claim 15, the combination of the structure comprising: "a pattern of mutually electrically isolated metal conductors disposed within said lower layer of dielectric material, said metal conductors comprising a plurality of spaced apart conducting regions extending to said upper surface of said lower layer, an upper layer of dielectric material disposed with a lower surface thereof in contact with and boded to said upper surface of said lower layer" (claim 1), "wherein said semiconductor device [disposed within said upper layer of dielectric material] is a field effect transistor comprising a first gate electrode in contact with one of said conducting regions at said upper surface of said lower layer" (claim 15) is not supported in the specification or drawing.

For example, Figs. 1-6B (first embodiment) does not show "a field effect transistor comprising a first gate electrode in contact with one of said conducting regions at said upper surface of said lower layer." And Fig. 7 (second embodiment) shows the semiconductor layer 57 in contact with and bond to the upper surface of the lower dielectric layer 52, but does not show

"an upper layer of dielectric material disposed with a lower surface thereof in contact with and bond to said upper surface of said lower layer", "wherein said semiconductor device is a field effect transistor comprising a first gate electrode in contact with one of said conducting regions at said upper surface of said lower layer".

- In claim 16, claim 16 is rejected because it depends on improper claim 15. Furthermore, the limitation of having "a second gate electrode is deposited upon said first insulating layer above each field effect transistor" is not supported in the specification or drawing.

2. Claim 32 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In claim 32, the limitation "each field effect transistor forms a memory element" is not supported in the original disclosure.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 11-12, 18, 26, 28-29, and 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Durlam et al's **Figs. 5-8** (US. 5,940,319).

Durlam's first embodiment (**Figs. 5-8**) discloses a substrate of semiconductor material; a lower layer (12a,21,25) of dielectric material disposed with a lower surface in contact with the substrate and an upper surface in spaced adjacency thereto; a pattern of mutually electrically isolated metal conductors 19a and 19b disposed within said lower layer of dielectric material, said metal conductors 19a and 19b comprising a plurality of spaced apart conducting regions extending to the upper surface of the lower layer, wherein each conducting region comprises a via (31,37) comprising electrically conducting material 37 formed on a barrier layer 31 of Ta (column 3, lines 35-42); an upper layer 51 of dielectric material disposed with a lower surface thereof in contact with and bonded to the upper surface of the lower layer; and a plurality of semiconductor device MTJs disposed within the upper layer of dielectric material 51, each of MTJs being in electrical contact with only one of the conducting regions at the upper surface of the lower layer.

5. Claims 26, 28 and 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Durlam et al's **Fig. 17** (US. 5,940,319).

Durlam's second embodiment (**Fig. 17**) discloses a microelectronic element array comprising: a semiconductor substrate 81; a first dielectric layer 86 formed on the substrate; a plurality of electrically isolated conductive regions disposed within the first dielectric layer 86, each conductive region comprising a conductive via (82,84) comprising a conductive material 82 formed on a barrier layer 84 of Ta; a second dielectric layer 96 having a lower surface which is bonded to an upper surface of the first dielectric layer 86; and a plurality of semiconductor nodes including a plurality of diodes and MTJs structure 93 and 92 formed in the second dielectric layer 96, each node being in contact with the via.

6. Claims 26, 28, and 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Gonzalez et al (US. 6,194,746).

Gonzalez (Fig. 30) discloses a microelectronic element array comprising: a semiconductor substrate; a first dielectric layer formed on the substrate; a plurality of electrically isolated conducting regions disposed within the first dielectric layer, each conducting region comprising a conductive via 162 comprising of tungsten (column 15, lines 38-45); a second dielectric layer 168 having a lower surface which is bonded to an upper surface of the first dielectric layer; and a plurality of semiconductor nodes of programmable resistor 164 formed in the second dielectric layer 168, each node being in electrical contact with the via.

7. Claims 26, 28 and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Aozasa et al (US. 6,054,734).

Aozasa (Fig. 23) discloses a microelectronic element array comprising: a semiconductor substrate 204; a first dielectric layer 206 formed on the substrate; a plurality of electrically isolated conductive regions disposed within the first dielectric layer 206, each conductive region comprising a conductive via 216 (column 4, lines 19-21); a second dielectric layer 244 having a lower surface which is bonded to an upper surface of the first dielectric; and a plurality of nodes comprising memory transistors 218 formed in the second dielectric layer 244, each node being in electrical contact with the via.

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 13-14, 17, 27, and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Durlam et al in view of Bronner et al (US. 6,242,770).

Durlam does not disclose that diodes are single crystal Si diodes.

However, it would have been obvious to form Durlam's diodes as single crystal Si diodes because according to Bronner, such single crystal Si diodes (column 9, lines 63-65) would provide high conductivity, high rectification and low total resistance (column 3, lines 1-4).

10. Claims 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Durlam et al in view of Oda (US. 5,994,749).

Durlam's first embodiment (**Figs. 5-8**) does not specifically disclose the metal conductor 19a being formed of a different material than the via 37.

However, Oda (Fig. 1) teaches the forming of a conductive contact structure comprising an aluminum layer 14 in electrical contact with the via 16 made of tungsten (column 5, lines 15-25) having low contact resistivity. Accordingly, it would have been obvious to form the metal conductor 19a and the via 37 of Durlam with the materials as set forth above because such contact structure is well known in the art for increasing the conductivity of the contact.

***Response to Arguments***

11. Applicant argues that the conductive region of the prior art does not include the via. However, Applicant's arguments are moot in view of the new ground(s) of rejection.

Applicant further argues that it is not obvious to combine Bronner with Durlam.

Applicant's arguments are not persuasive because the motivation of providing high conductivity, high rectification and low total resistance resulted from a diode made of

monocrystalline silicon material as suggested by Bronner would motivate one skilled in the art to combine the references.

***Conclusion***

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (703) 308-4917. The Examiner can normally be reached on Monday through Thursday. If attempts to reach the Examiner by telephone are unsuccessfully, the Examiner's supervisor, Wael Fahmy, can be reached on (703) 308-4918.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. Group 2800 fax number is (703) 308-7722 or (703) 308-7724.

PC
March 23, 2003

PHAT X. CAO
PRIMARY EXAMINER